



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/789,605

02/27/2004

Hanfang Pan

030475

9037

23696

7590

08/22/2006

QUALCOMM INCORPORATED  
5775 MOREHOUSE DR.  
SAN DIEGO, CA 92121

EXAMINER

TORRES, JOSEPH D

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/789,605

Applicant(s)

PAN ET AL.

Examiner

Joseph D. Torres

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15, 20 and 23-36 is/are rejected.
- 7) ☒ Claim(s) 16-19, 21 and 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. In view of the amendment filed 07/25/2006, the Examiner withdraws all previous rejections under 35 USC § 112.

### ***Claim Rejections - 35 USC § 101***

2. In view of the amendment filed 07/25/2006, the Examiner withdraws all previous rejections under 35 USC § 101.

### ***Response to Arguments***

3. Applicant's arguments filed 07/25/2006 have been fully considered but they are not persuasive.

For the purposes of responding to the Applicant's arguments, the Examiner rewrites the previous rejection to claims 1, 29, 30, 35 and 36, below specifically to address newly amended language:

Kaul teaches a mapper receiving at least one pair of received symbol values (serial to parallel converter S/P 200 in Figure 5 in Kaul receives a pair of sub-bursts, one sub-burst from channel A and another sub-burst from channel B and maps serially transmitted burst data to parallel data; the serial to parallel converter S/P in Figure 5 is a mapper; Note: sub-bursts from channel A and channel B are mapped to a pair of

Art Unit: 2133

parallel outputs, one pair of the parallel outputs comprising even burst values and the other pair of the parallel outputs comprising odd burst values), each pair of received sub-burst symbol values comprising a first value and a second value (Note: a sub-burst comprises at least a first value and a second value), and generating a plurality of third values in response to at least one pair of received symbol values (serial to parallel converter S/P 200 in Figure 5 in Kaul generates a pair of parallel outputs, one pair of the parallel outputs comprising even burst values and the other pair of the parallel outputs comprising odd burst values; the pair of parallel outputs are a plurality of third values generated in response to the received pair of channel A and B symbol sub-burst values);

a plurality of memory banks, each memory bank adaptable to store one of the third values (Memory Banks 201A and 201B in Kaul are a plurality of memory banks, each memory bank adaptable to store one of the parallel-mapped third values; Note: Memory Bank 201A stores the even burst values from the pair of parallel output third values and Memory Bank 201B stores the odd burst values from the pair of parallel output third values); and a controller for directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern determined to allow for de-interleaving by retrieving values from the plurality of memory banks (col. 9, lines 32-68 in Kaul teaches that Address Controller 205 in Figure 5 is a controller for directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to

an even and odd storing pattern, the storing pattern determined to allow for de-interleaving by retrieving values from the plurality of memory banks).

The Applicant contends, "Kaul does not teach simultaneous storing, according to a storage pattern, of the third plurality of storage values".

Col. 9, lines 52-54 in Kaul explicitly teaches that both memories are simultaneously controlled during write so the writing of odd sub-bursts and even sub-bursts is performed simultaneously. Sequential writing of odd sub-bursts to the first memory and even sub-bursts to the second memory is a storage pattern for the pair of parallel output third values.

The Applicant contends, "Applicant traverses the claim that the S/P block serves as the mapper".

The Examiner asserts that the Authoritative Dictionary of IEEE Standards Terms defines map as established correspondence between elements of one set and element of another set. The serial to parallel converter S/P 200 in Figure 5 of Kaul deterministically establishes a functional correspondence between serial input bursts and parallel output of burst data. The serial to parallel converter S/P 200 in Figure 5 of Kaul is a map by definition.

The Applicant contends, "With respect to claim 5, Applicant is unclear on the meaning of the Examiner's note".

Third values in Figure 5 of Kaul are comprised of two parallel sets of lines one set of parallel lines for even sub-burst data and the other set of parallel lines for odd sub-burst data. There are four memory banks twice as many as the pair of parallel output lines from serial to parallel converter S/P 200 in Figure 5 of Kaul.

° The Applicant contends, "The Examiner's response is unclear as to the grounds for rejection for claims 20 and 33".

As per claim 20:

Kaul teaches a two-cycle even and odd pair wise storage pattern for each encoded frame/burst from the encoder in Figure 2 (Note: and encoded frame is encoding sequence pattern).

As per claim 33:

Kaul teaches simultaneously retrieving two or more stored third values from two or more memory banks according to a retrieval address (the MUX for Memory Banks 201A and 201B in Figure 5 of Kaul retrieves two or more stored third values from two or more memory banks according to a retrieval address); and incrementing the retrieval address sequentially subsequent to a simultaneous retrieval (col. 9, lines 62-64 in Kaul teach sequential extraction of data).

The Applicant contends, "With respect to claims 14, 15, 20, 21, 23, 24, and 31-34, the Examiner makes a §103(a) rejection based solely on the Kau] reference. However, Kaul does not teach each of the limitations of these claims".

The Examiner disagrees.

As per claim 14:

Kaul teaches a pair wise even and odd storing pattern comprising a pair of cycles, each cycle indicating; a selected subset of the plurality of memory banks (For example an odd cycle indicates one of the banks for storing odd bursts is selected) and an address offset value for each memory bank in the selected subset (col. 9, line 53-55 in kaul teach sequential writing so the offset is one), each of the memory banks in the selected subset for storing one of the plurality of third values, respectively (Memory Bank 201A stores the even burst values from the pair of parallel output third values and Memory Bank 201B stores the odd burst values from the pair of parallel output third values).

As per claim 15:

Kaul teaches the bank selection, offset selection, and third value selection are assigned in accordance with an encoding sequencing pattern (Figure 2 teaches that interleaved data is encoded so that even and odd sub-bursts comprise encoded data so that bank selection, offset selection, and third value selection is explicitly performed on an encoding sequencing pattern; Note: and encoded sub-burst is an encoding sequencing pattern). Note: Kaul teaches a pair wise even and odd storing pattern comprising a pair of cycles, each cycle indicating; a selected subset of the plurality of memory banks (For example an odd cycle indicates one of the banks for storing odd bursts is selected) and an address offset value for each memory bank in the selected subset (col. 9, line 53-55 in kaul teach sequential writing so the offset is one), each of the memory banks in the selected subset for storing one of the plurality of third values, respectively (Memory

Art Unit: 2133

Bank 201A stores the even burst values from the pair of parallel output third values and Memory Bank 201B stores the odd burst values from the pair of parallel output third values).

As per claim 20:

Kaul teaches a two-cycle even and odd pair wise storage pattern for each encoded frame/burst from the encoder in Figure 2 (Note: and encoded frame is encoding sequence pattern).

As per claim 23:

Kaul teaches a pair wise even and odd storing pattern comprising a pair of cycles, each cycle indicating; a selected subset of the plurality of memory banks (For example an odd cycle indicates one of the banks for storing odd bursts is selected) and an address offset value for each memory bank in the selected subset (col. 9, line 53-55 in kaul teach sequential writing so the offset is one), each of the memory banks in the selected subset for storing one of the plurality of third values, respectively (Memory Bank 201A stores the even burst values from the pair of parallel output third values and Memory Bank 201B stores the odd burst values from the pair of parallel output third values).

Note: a current address serves as a base address until it is incremented.

As per claim 24:

The process is same is identically repeated for every burst. The address must be re-initialized to place the first data in the correct location.

As per claim 31:

Claim 31 comprises substantially the same limitations as in claims 14, 15 and 23.



Art Unit: 2133

As per claim 32:

Claim 3 comprises substantially the same limitations as in claim 14.

As per claim 33:

Kaul teaches simultaneously retrieving two or more stored third values from two or more memory banks according to a retrieval address (the MUX for Memory Banks 201A and 201B in Figure 5 of Kaul retrieves two or more stored third values from two or more memory banks according to a retrieval address); and incrementing the retrieval address sequentially subsequent to a simultaneous retrieval (col. 9, lines 62-64 in Kaul teach sequential extraction of data).

As per claim 34:

Col. 10, lines 6-10 in Kaul.

The Examiner disagrees with the applicant and maintains all rejections of claims 1-15, 20 and 23-36. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that claims 1-15, 20 and 23-36 are not patentably distinct or non-obvious over the prior art of record in view of the references, Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) in view of Jeong; Gibong (US 6907084 B2) in view of Ross; Daniel P. (US 4901319 A) in view of Khayrallah; Ali S. et al. (US 6798852 B2, hereafter referred to as Khayrallah) in view of Zehavi; Ephraim (US 6496543 B1) in view of Shiu; Da-shan et al. (US 6392572 B1, hereafter referred to as Shiu) as applied in the last office action, filed 04/25/2006. Therefore, the rejection is maintained.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5, 6, 25, 28-30, 35 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 2-4 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) in view of Jeong; Gibong (US 6907084 B2).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) in view of Ross; Daniel P. (US 4901319 A).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

7. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) and Ross; Daniel P. (US 4901319 A) in view of Jeong; Gibong (US 6907084 B2).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) and Ross; Daniel P. (US 4901319 A) in view of Khayrallah; Ali S. et al. (US 6798852 B2, hereafter referred to as Khayrallah).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

Art Unit: 2133

9. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) and Ross; Daniel P. (US 4901319 A) in view of Zehavi; Ephraim (US 6496543 B1).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) in view of Shiu; Da-shan et al. (US 6392572 B1, hereafter referred to as Shiu).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

11. Claims 14, 15, 20, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

12. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) and Jeong; Gibong (US 6907084 B2) in view of Khayrallah; Ali S. et al. (US 6798852 B2, hereafter referred to as Khayrallah).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

13. Claims 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

14. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) in view of Jeong; Gibong (US 6907084 B2).

See the Non-Final Action filed 04/25/2006 for detailed action of prior rejections.

#### ***Allowable Subject Matter***

15. Claims 16-19, 21 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

Art Unit: 2133

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



JOSEPH TORRES  
PRIMARY EXAMINER

Joseph D. Torres, PhD  
Primary Examiner  
Art Unit 2133